Construction Project:

A PC-BASED 32CH LOGIC ANALYSER - 2

Here's the second of two articles describing this new instrument, which offers sampling at up to 40MHz and fully maskable 32-channel triggering — all under software control. In this article the authors cover its construction, testing and use.

by DAVID L. JONES and DAVID BULFONI

The PCLA has been designed to be as easy to assemble as possible. All of the components, with the exception of the D25 connector, transformer, and two LEDs are mounted on a single sided PCB measuring 230mm x 115mm.

The project is neatly housed in an instrument case measuring 260 x 180 x 65mm. The PCB is butted up against the front panel, to allow the right-angle mounting test probe connectors to protrude from the front panel, eliminating any internal cabling. The only other components mounted on the front panel are two LEDs — one for power, and the other for data indication. A combined IEC mains input connector and fuseholder, along with a DB25 connector for the cable to the PC, are the only items mounted on the back panel.

After checking the PCB for the usual etching problems, work can commence on PCB assembly by installing the 50 or so wire links required. It pays to keep some of the longer links as straight as possible, to make the board look much neater. Take note of the angled link between the crystal and IC5.

Install the three resistors and five resistor packs next. Don't confuse RP1 (1k) with the other four 100k networks, and be sure to match the 'common' end of each network with that marked with a square on the overlay.

Now come all of the IC sockets. It is highly recommended that all of the ICs be mounted in sockets, especially the input latches and the RAMs. Using sockets, the repetitiveness of the circuit will make troubleshooting much easier at a later stage. About the only IC's which aren't either expensive or connected to an outside circuit which can cause damage are ICs 3, 4, and 5.

It may be difficult to obtain the 28-way 'skinny DIP' sockets required for the RAMs, but in this case two 14-pin sockets can be connected end to end. In fact, two 14-pin sockets may also be cheaper than one 28-way one.

The three 44-way PLCC sockets rate a special mention. Due to Murphy's law, it is extremely easy to solder in a PLCC socket the wrong way around! A PLCC chip will only go into the socket in one of the four possible orientations, so it is vital to get the socket around the correct way.

The PLCC socket has a bevelled edge on one corner, and this must match the bevelled edge on the component overlay. Also make sure that all of the pins protrude through their holes. If you are using a homemade PCB and drill a few holes off centre, then it can be very frustrating trying to insert the socket!

Install all of the capacitors next, with the exception of C1. Watch the orientation of the two tantalum capacitors. Also install the five PCB stakes and bridge rectifier.

Next comes the three IDC connectors CN1, CN2, and CN3. The best way to install CN3 is to keep the header plug attached to the header pins. This will keep the header pins straight and aligned while they are being soldered. CN1 and CN2 should also be bolted to the PCB with M2.5 nuts and bolts. This will stop pressure from being exerted on the solder joints when the test probe leads are connected and disconnected from the front panel.

Lastly, install C1 and the regulator. Bolt the regulator and heatsink to the PCB before soldering the leads.

Attention can now be turned to the mechanical side of things. If you don't have pre-punched panels, then cutouts will need to be made for the mains connector, DB25 connector, the LEDs and probe connectors. The only cutouts which will need alignment are those for the probe connectors. The probe cutouts can extend down to the bottom of the panel if you wish, but some may prefer to take a bit more time to make the cutouts only just big enough to accept the connector.

Holes will also need to be drilled for the PCB and transformer. The PCB should be as close to the front panel as possible, to allow the probe lead connectors to extend out. The PCB is just wide enough to fit between the two front support posts.

The transformer should be mounted in the middle of the back part of the case, with the mains input towards the rear panel. Securely connect the transformer frame to the main earth pin on the IEC socket. All mains wiring connections should be properly insulated with electrical tape and heatshrink.

Connect the 8.5V winding of the transformer to the AC input pins on the PCB, and connect the LEDs to their respective PCB pins.

The LEDs can now be wired to the PCB. Only three wires are required for this, one for the anode of each LED and their common ground connection. The cathode of both LEDs will have to be connected together on the front panel and connected to the ground lead.

Finally, assemble the IDC female DB25 connector and 26-way IDC header to a short length of ribbon cable, just long enough to connect from the PCB to the rear panel.

Before installing any of the ICs, apply power and ensure that 5V is available on the supply pins of each IC socket. The power LED should also be on. Disconnect the power, and install all of the ICs — paying close attention to the correct orientation. Be sure to use relevant anti-static procedures to avoid damaging any of the ICs. The LSI devices will be labeled 'LACC', 'LATC1' and 'LATC2'. Ensure that these devices are installed in their correct sockets as follows: LATC1 is IC14, LATC2 is IC15 and LACC is IC16.

Carefully check the orientation of

each LSI device before pushing it down into the socket. The bevelled corner on the chip must match the bevelled corner on the socket. Trying to force the chip in with the wrong orientation may damage the IC and socket pins.

Re-apply the power and check the 5V supply rail on all of the chips. If the heatsink gets overly hot, then something may be loading down the supply. If this is the case, then it is likely to be a PCB short somewhere. Start by removing the ICs one by one and repowering until you track down the fault.

Assuming that the hardware hasn't gone up in smoke, it's time to connect the PCLA to the PC. Use a 25-way ribbon cable with a DB25 IDC male on one end, and a DB25 IDC female on the other end. In fact, it is best to make up a 'universal' cable with both female and male DB25 connectors and a 26-way IDC DIL header on each end. This will also you to use the cable for all sorts of other projects as well. The cable should be kept as short as possible, with an absolute maximum length of about two metres.

Probe construction

One of the most difficult and expensive parts of building a logic analyser would have to involve the test probes. Unlike an oscilloscope or multimeter, the PCLA has 32 inputs, and if you want to fully use all 32 channels, then you will have to make 32 or more test probes!

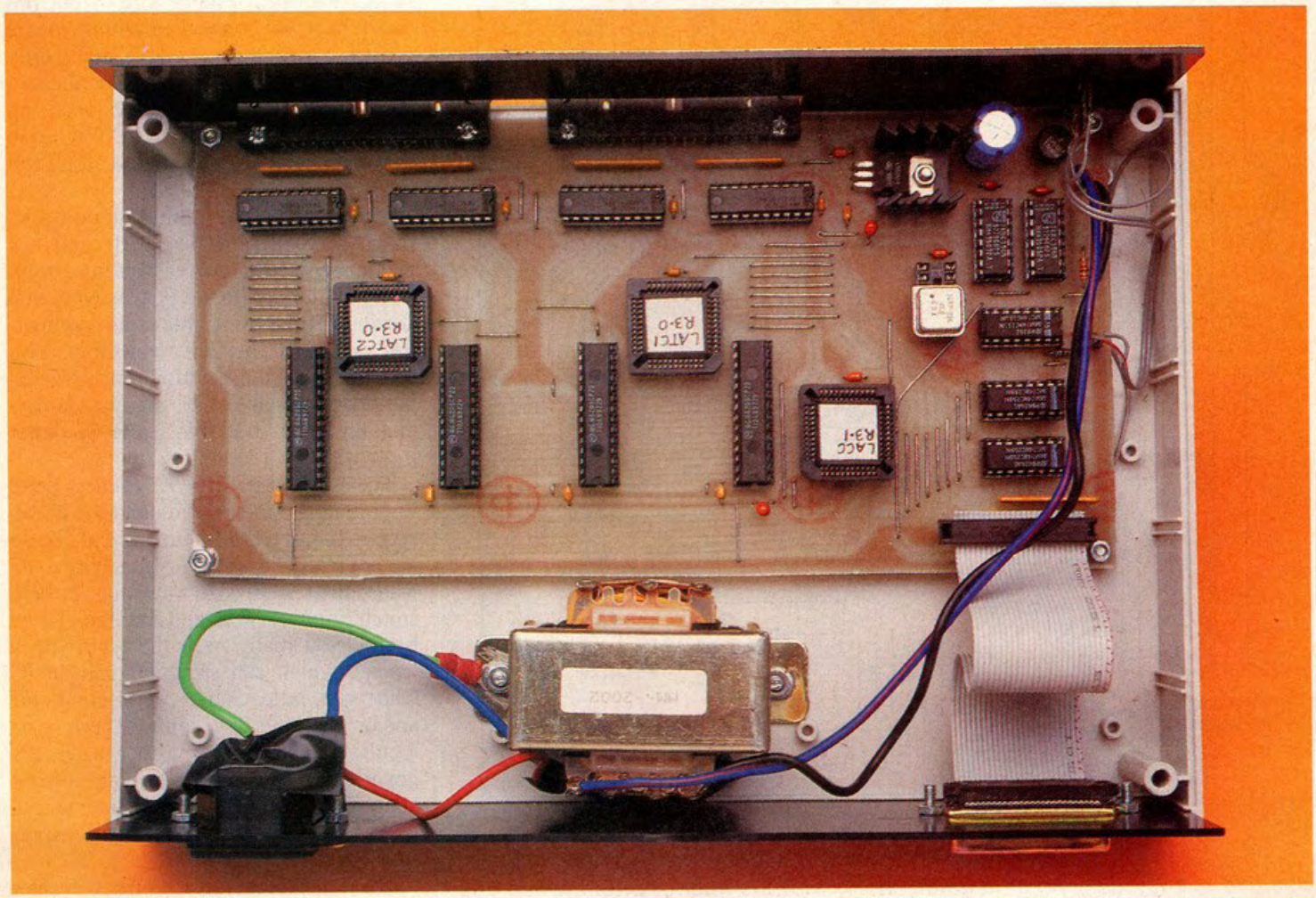
Like most commercial logic analysers, the PCLA uses levered dual row IDC header connectors for the probe inputs, which provides a low cost and compact solution. Unfortunately, there is no standard pinout or connector size for logic analysers. Almost every manufacturer uses their own custom pinout, so don't rush out and buy a set of Joe Blow logic analyser probes...

The PCLA has two 34-way connectors which provide all of the 32 channel inputs, external clock, external trigger, ground and an external +5V supply signals. The front panel label shows the pinouts of the two connectors. The pinouts are the same for pins 1-32 on both connectors, but pins 33 and 34 differ. One connector provides the clock and trigger inputs, while the other provides a +5V output on both pins.

So what kind of probes do you need? It all depends on what you want to measure. The photographs show two of the most common types of probes. One of them uses a commonly available 16-way DIL test connector, which simply clips over a DIL IC in-circuit. This sort of probe is useful for quick testing of all the pins on a single IC.

The prototype of this probe used 8-way SIL header connectors to allow easy disconnection of the test head. The SIL connector can then be used as a test head in its own right, but this makes it rather difficult to connect an external clock to one of the pins. If you need to easily connect the external clock, then it is much simpler to solder the wires directly onto the test head pins. This allows you to connect a clock line using an EZ-HOOK.

It might be wise to make up a 28-way, 20-way, 16-way and 14-way version of this test head, for general testing of ICs. With 32 channels available on the PCLA, two 16- or 14-way test heads can



Inside the new Logic Analyser. Thanks to the use of three preprogrammed PLD chips, everything fits on a single-sided PC board. The input probe leads connect directly to the two 34-way IDC DIL connectors visible at the upper left, which protrude through the front panel.

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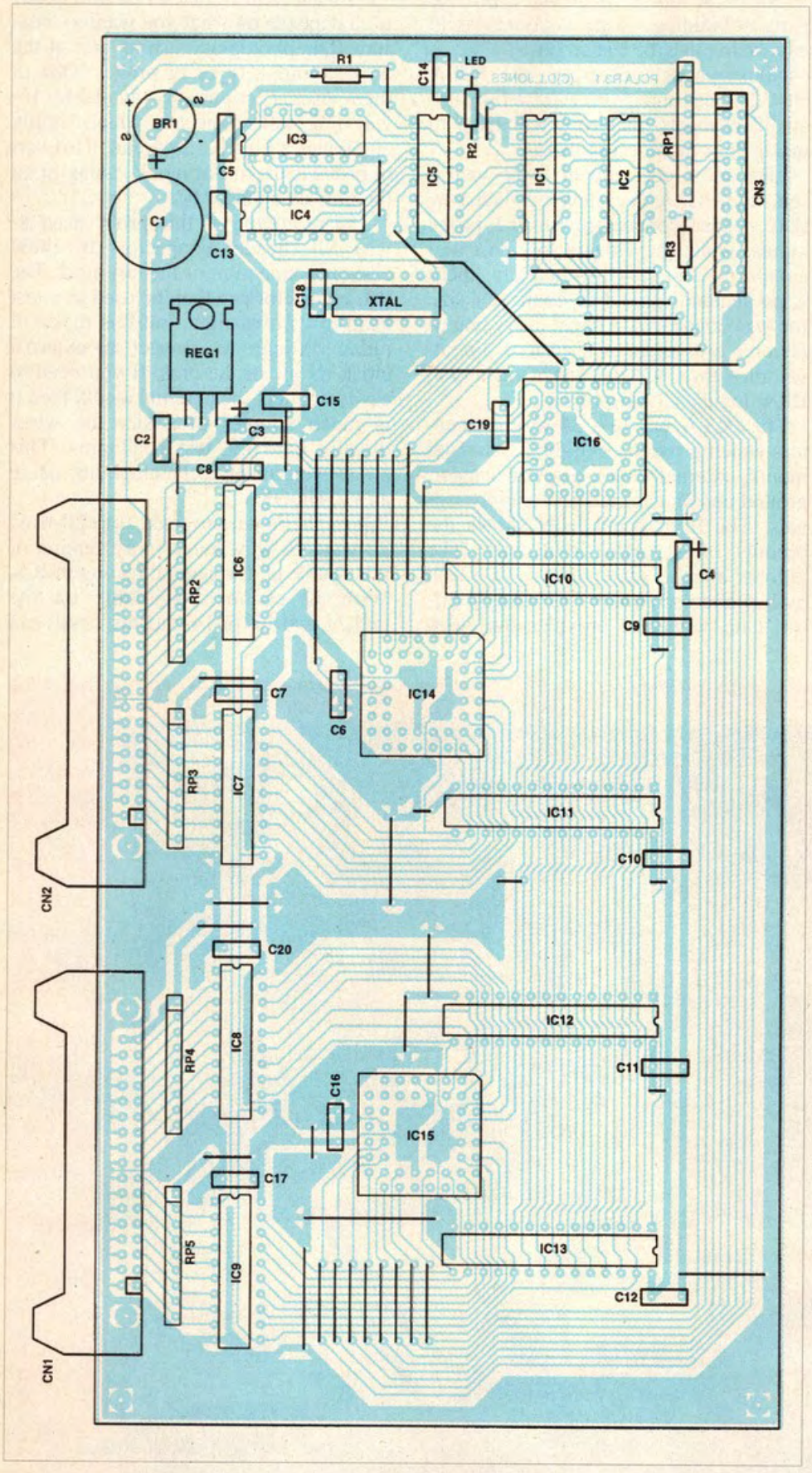


Use this overlay diagram as a guide, along with the interior photo, when you are wiring up the PCB for your own analyser. The author recommends that sockets are used for all ICs, and suggests that you take particular care with the orientation of the sockets for the PLD chips IC14, IC15 and IC16.

be used at the same time.

When making one of these connectors, it is recommended to match the actual IC pin number with the corresponding input channel on the PCLA connector. This just makes it a lot easier to remember which input goes to which pin, when using the software.

The other photograph shows a 16-channel EZ-HOOK test probe. I actually had a good quantity of these premade leads in my junk box from an old logic analyser, complete with 'claw' type EZ-HOOKs. They used 10-pin header connectors, so I just snipped off the connector and attached the individual leads to a short length of ribbon cable. The probes are arranged in the resistor colour code sequence to aid in identification.

You can make your own EZ-HOOK probes using a 34-way IDC DIL header plug, about 300mm of ribbon cable and a few dozen EZ-HOOKs. It's a simple matter of connecting the IDC connector to the ribbon cable, and then connecting an EZ-HOOK to each input wire.

When splitting the cable into individual wires, leave a ground wire attached to the side of each input wire — but you don't have to connect anything to the ground wire at the test end. Usually only one ground wire is enough to connect to the circuit, although you can make up extra ground leads if you like. Also make up leads for the external clock and trigger inputs.

If you don't use multi-colour cable, then you will have to label each test probe with the corresponding input channel number on the PCLA. Note that standard 'rainbow' cable is not compatible with IDC header connectors. You can also use the multi-colour 'twisted pair' ribbon cable like many commercial units do, but this cable is rather more difficult to obtain.

The type of EZ-HOOK used is quite important. I don't recommend the cheap type with just a 'hook' on one end. These are not really designed for attaching to IC leads; their large size only makes them suitable for resistors and the like. To be useful, you really need the type with a 'claw', which can securely grab an IC lead with little chance of slipping off and/or shorting two pins. These type aren't exactly cheap, but then again it's never going to be cheap to build a logic analyser probe! If you want to make a good range of test probes, then be prepared to spend over $100.

These general purpose probes will cater for most of the common circuits, but if you want to test surface mount or large PLCC packages, then you'll have little

choice but to make up specialised probes.

It may be handy to make up some probes with a two-pin header on each of the channels. This is a common type of probe used in a lot of commercial equipment. In fact, many designs have built-in logic probe test points, usually of the two-pin header variety, where one wire is the signal, and the other a ground.

If you are designing a circuit of your own and think you may use the logic analyser for evaluation or troubleshooting, then it is a wise idea to add some two-pin header logic probe test points. As header connectors are very cheap, the main problem will either be lack of space for the connector, or lack of room to route the tracks to the connector.

If you've ever seen a commercial PCB with rows of unused two-pin connectors, or PCB pads without any connector, you'll now know what they are for!

Who knows, the way things are going, TV and VCR service manuals of the future may have logic diagrams instead of CRO shots...

Taking measurements

Using a logic analyser has many traps for the unwary. Unlike an oscilloscope, there is no easy way to tell what effect adding the logic probe to a circuit makes. The only output you have is either HIGH or LOW, and if you don't know exactly what the circuit is supposed to do, then you have little choice but to trust the logic analyser.

There are however two problems which are the most common and easy to look out for. One is the use of the PCLA at high speeds (greater than a few MHz), and the other involves data misinterpretation at the sampling point.

The first problem, of high speed operation, is fairly obvious. Usually when taking high speed measurements with an oscilloscope, a x10 probe is used. This provides a much lower probe capacitance and hence less disturbance of the circuit under test. The PCLA doesn't have the same capability of using a x10 low capacitance probe, and all measurements are taken with a directly connected input. In our case, we're using a 74ACT series gate. Here the amount of probe capacitance will depend on the length and type of cable being used.

The probe capacitance has a dramatic loading effect on high speed circuits, so this is something to be wary of if you are not getting the result you expect.

The rule is to either keep the cable as short as possible —generally less then 300mm — or to use a buffered probe. A buffered probe is an external box with a buffer chip as close to the probe inputs as possible. You can then use a much longer cable to connect to the PCLA. The PCLA provides a +5V output which can be used to power external buffer probes.

Another use of a buffer probe box is to provide different types of input matching. The PCLA has 74ACT series logic on the input, and can therefore accept either TTL or 5V CMOS signal levels. If you want to measure 4000 series logic of a higher voltage, or the newer 3.3V logic, or even ECL, then you will have to make an appropriate buffer box. The box should convert the incoming signal to a TTL level acceptable for the PCLA.

The second problem concerns the fact that the PCLA has to 'latch' the data at some discrete point. If the input happens to be changing from one state to another at this same point, then the PCLA will not register the data correctly and may interpret the data as either logic level. This can readily be seen by measuring a constant square wave of lower frequency than the internal sample clock.

Say for example that the input is a constant 10MHz square wave, and the PCLA is using its internal clock of 40MHz. In this case you would expect to see the captured waveform change state every four clock samples, and this is what you get — most of time!

Every so often, the input may change state right at the point the data is clocked into the latch. If the latch misinterprets the data, then the display will show the input pulse longer or shorter than it really is. There is no real way to avoid this when using the internal PCLA clock (TIMING mode), so be wary of it.

In effect, this is similar to the quantisation error in A to D converters. Just as they can only measure a finite number of levels, so too the PCLA in TIMING mode will always have a probable error of one sample clock period.

A similar problem exists in STATE analysis mode, but this time it is possible to prevent it. Because the external clock on the PCLA has to pass through IC5 and the control chip, it will inevitably have some delay or 'skew' associated with it compared to the input data.

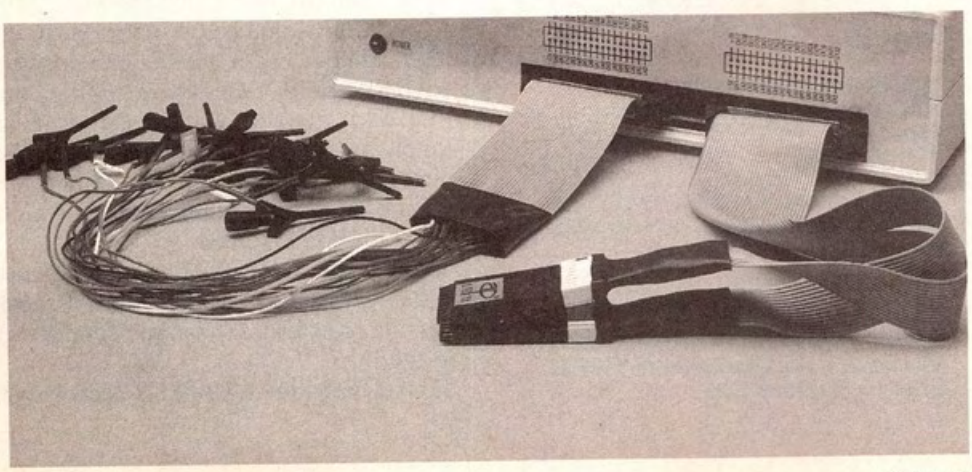
If you are not getting the results you expect in STATE mode, then try inverting the external clock polarity in the software. This will usually fix the problem, but at high speeds the skew may be too much to capture data reliably. This is why the PCLA is arbitrarily limited to a speed of 20MHz in STATE analysis mode.

You can push the speed to the full 40MHz if you feel confident enough that the clock skew will not be a problem. Alternatively, you can use an external buffer probe to try and delay the data to match the delay of the clock. But you're on your own with this one!

Expensive commercial units get around the problem by switching the external clock straight through to the latch clock input. However, adding this feature to the PCLA would have overly complicated the design.

It is also important to select a proper ground when measuring high speed signals. In such circuits, moving the ground lead just a few inches can add significant 'ground bounce' to the signal being measured. Although this is more important (vital!) with an oscilloscope than a logic analyser, it's still something to watch out for. It's always good practice to connect to the ground pin of the chip you are testing.

The PCLA triggers off data fed from the input latches. This means that the PCLA does not have any 'glitch capture' capability like some of the more expensive commercial logic analysers. This may be a problem if you are looking for a particular fault which may only occur for a short period of time. If you



For general work, two different kinds of input probe are most useful: a set of individual EZ-HOOK leads like those at left, and a 16-pin DIL IC clip like that at right.

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set the PCLA to trigger off the fault condition then depending on the sample rate, the input can match the fault condition, but if the data is not being latched and sampled at that time, the trigger circuit will never see it.

However, there is a partial solution to this. The 74ACT574 input latches can be replaced with 74ACT573 transparent latches. These will allow the data inputs to pass 'transparently' through the latch when the clock input is HIGH. This will at least give the PCLA glitch capture capability for at least half of the sample clock, which is better than nothing. The 573's will latch the data on the negative edge of the clock, but this is the same time as the data is written into the RAM. If the data changes just before the latching takes place, then the RAM may not have enough setup time required to successfully write the data into the RAM.

Using the 573's was the original intention for the PCLA, but the prototype proved a bit touchy at the higher sample rates. But if you're after a glitch capture capability, then this may be a worthwhile modification.

To design the PCLA to incorporate full glitch capture capability would have required the trigger inputs to be permanently connected to the inputs. This would require a set of buffer chips, and certainly a double-sided PCB.

Frankly I don't believe the lack of a glitch capture capability is a major disadvantage in a low cost design such as this. In fact, it's sometimes beneficial to have a design that will ONLY trigger off the data that is actually captured and displayed.

Using the software

The minimum requirements for the software are a DOS based 286 or higher IBM compatible, with a VGA screen and parallel port. Any standard printer which supports the IBM extended character set can be used for hardcopy printout, as the software prints using text mode. It is recommended to use a second parallel port if the printer is to be used at the same time as the PCLA.

After installing the software, start the program by running the PCLA batch file. A main menu will appear with the various options in the middle of the screen, and the channel information box on the left hand side.

The channel information box will always remain on screen, and provides the channel number, on/off control, trigger setting, channel type, and user defined label for each of the 32 channels.

The main menu provides the following options :

TIMIMG DISPLAY: This displays a timing diagram waveform view of the most recently captured data. It allows you to zoom and expand the waveform window, and scroll the entire 32KB buffer on all 32 channels. Two cursors are available to measure the time interval and number of clock periods between two points.

DISASSEMBLY DISPLAY: This routine decodes the most recent data into separate address and data fields specified by the channel type information. This is used for decoding microprocessor buses and the like. The information is display in two columns, one containing the address, and next to it the data.

CAPTURE DATA: Starts the PCLA sampling data using the current trigger information and options specified. It then retrieves the data from the PCLA after sampling has finished. The DATA LED on the front panel will change state according to what the PCLA is doing. During PRE-TRIGGER sampling, the LED will be fully ON. During data retrieval the LED will be blinking rapidly at half brightness, and the LED will be OFF when data retrieval is complete.

EDIT DATA: Allows editing of all the trigger and channel options. The USED check box turns each channel on and off. Turning off a channel will only stop it from being displayed, but it will still be retrieved and triggered from. Any unused channels should be turned off, as this will speed up the display refreshing.

The trigger check box can be set to HIGH, LOW, or DON'T CARE. This sets the desired trigger setting for that channel. Remember to set all unused channels to DON'T CARE (X). The default state is DON'T CARE for all of the channels.

The TYPE box allows the user to define that channel as a particular data bit or address bit, for use with the disassembly function. Both address and data can be up to 31 bits wide. You do not need to specify all of the bits for the disassembly function to work; you can skip unused bits and only specify the ones you are interested in. For example, you may only want to decode address bits 2, 5, 6, 7 and the first four data bits.

An eight-character user defined label can be set for each channel in the LABEL field. Whenever using the PCLA, it's worth taking the time to label all used channels, as it can become very difficult to remember which input you connected to which point on your circuit.

TRIGGER SOURCE: This selects either internal (from the word trigger circuit) or external (from the connector) triggering.

TRIGGER POLARITY: Selects either

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PARTS LIST

Semiconductors

IC1,2	74HCT259 8 bit adressable latch
IC3,4	74HC390 dual decade counter
IC5	74AC151 8 bit multiplexer
IC6-9	74ACT574 octal 3-state latch (or 74ACT573 — see text)
IC10-13	32Kx8 20ns cache SRAM (any brand) (skinny DIP package as used on PC motherboards).
IC14	ispLSI1016-80 (LATC1_30.JED)*
IC15	ispLSI1016-80 (LATC2_30.JED)*
IC16	ispLSI1016-80 (LACC31.JED)*
REG1	7805 (TO-220) 5V regulator
DB1	WO4 1A diode bridge
XTAL	40MHz TTL XTAL oscillator (8/14 pin DIL)
L1	5mm green LED
L2	5mm red LED

Resistors

R1	100k 0.25W 5%
RP1	1k x 7 SIP network
RP2-5	100k x 8 SIP network

Capacitors

C1	2200uF 16V RB electrolytic
C3,4	10uF 10V tantalum
C2,5-20	0.1uF 0.2 pitch monolithic ceramic

Miscellaneous

2115 type 8.5V 1A mains transformer
PCB, single sided (PCLA31)
DB25 female IDC connector
100mm length of 25-way ribbon cable
ABS case, 260 x 180 x 65mm (W x D x H), Jaycar type HB5984 or similar
Small fined TO-220 heatsink
Three 44-way PLCC sockets; eight 14-way DIL sockets; five 16-way DIL sockets; four 20-way DIL sockets; two 34-way R/A IDC levered headers; one 26-way dual row straight pin header; one 26-way IDC header plug; two 5mm LED bezels; six M3 nuts, bolts and washers; four M2.5 nuts and bolts; one IEC mains cord; set of four PCB mounting spacers; fused panel mount IEC mains connector; tinned copper wire; mains rated hookup wire; solder, etc.

PLD, Software availability:

*The programmed logic devices used in this project (IC14, 15 and 16), and also the PC software needed to control it, are available from Tronnort Technology, of 12 Copeland Road, Lethbridge Park 2770. The quoted prices (including postage within Australia) are:

Software only.....$35
Three programmed 1016 PLDs.....$55
Software and programmed PLDs.....$80

Tronnort Technology can accept phone/fax orders and/or enquiries only after business hours, on (02) 9628 1223.

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positive or negative triggering when external triggering is selected. This setting will automatically be set to positive when internal triggering is selected.

TRIGGER DELAY: A trigger delay of 0, 2, 4 or 8 cycles is selectable. This determines how long the trigger signal must be present in order for the PCLA to register the trigger event. It can be used to avoid false triggering, and also for a legitimate use when you want to distinguish between short and long trigger events.

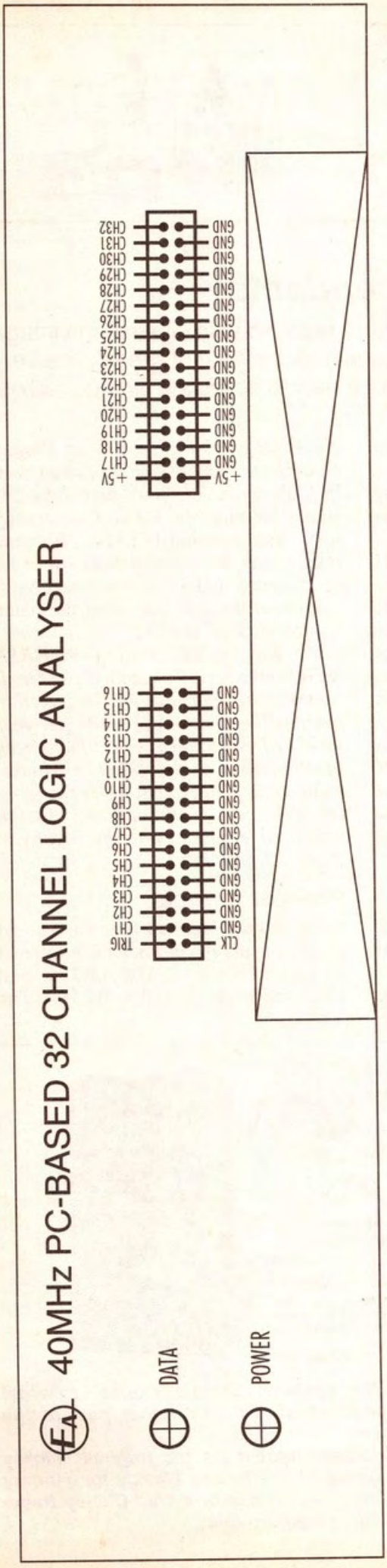
CLOCK SELECT: Toggles through all of the internal TIMING mode clock sample rates, and also selects the STATE mode external clock.

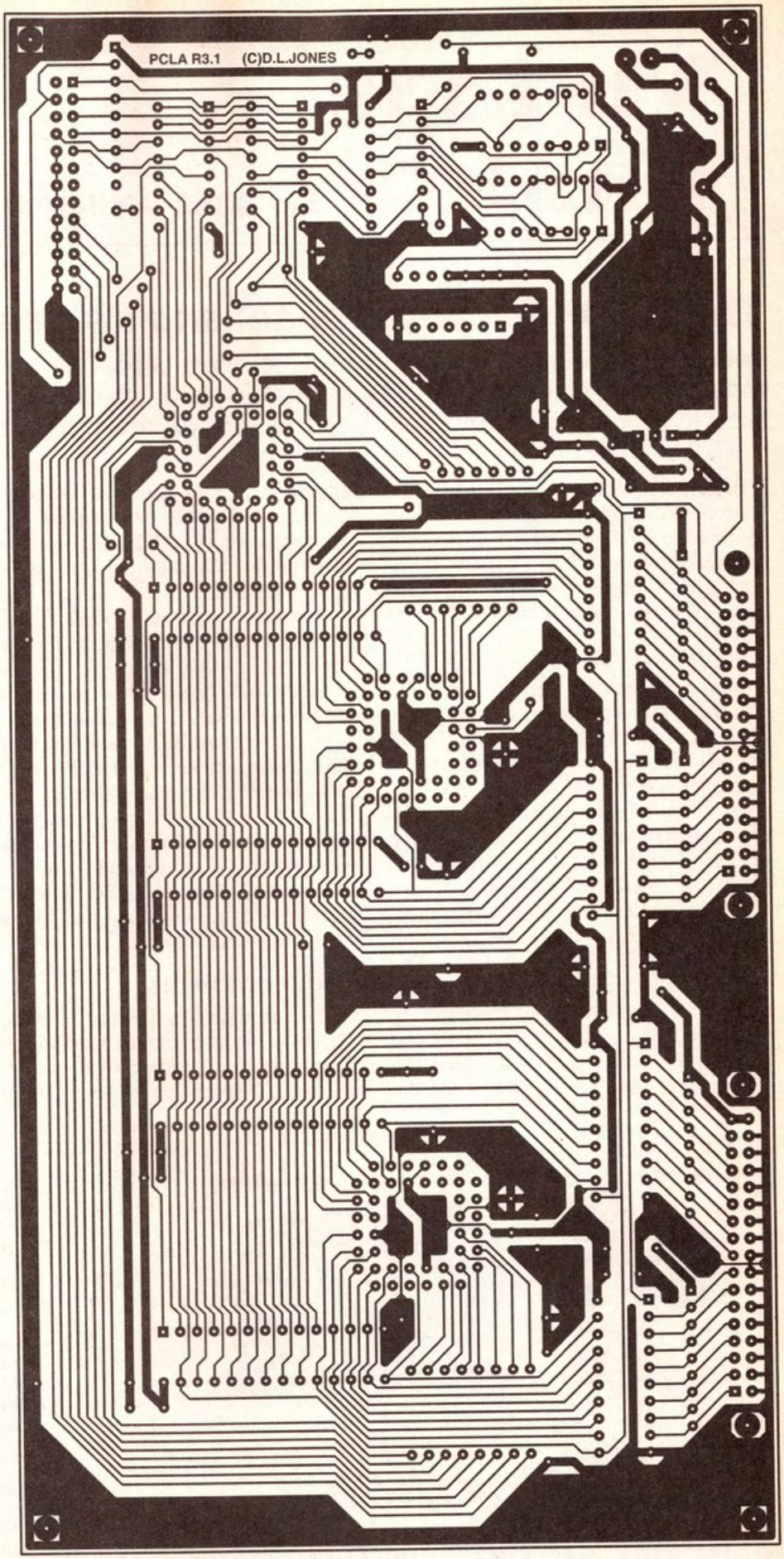
CLOCK POLARITY: Determines if the data will be sampled on the positive or negative edge of the external clock. This has no effect when in TIMING mode.

That's about all there is to the software. As you can see it's quite straightforward. Further information is available in the software documentation provided on the disk.

The software and pre-programmed PLDs will be available from Tronnort Technology. Please refer to the note in the parts list for more details.

That brings to an end the description of the new PC based logic analyser. I hope you find it a valuable addition to your test gear collection. Happy triggering! ❖





Here is the artwork for the Logic Analyser's front panel (left) and the PCB (above), reproduced actual size for those who like to make their own. The large rectangular area on the front panel with crossed diagonal lines is for the input connector cutout.